OIPE IAP4C
AUG 11 2006
PATENT & TRADEMARK OFFICE

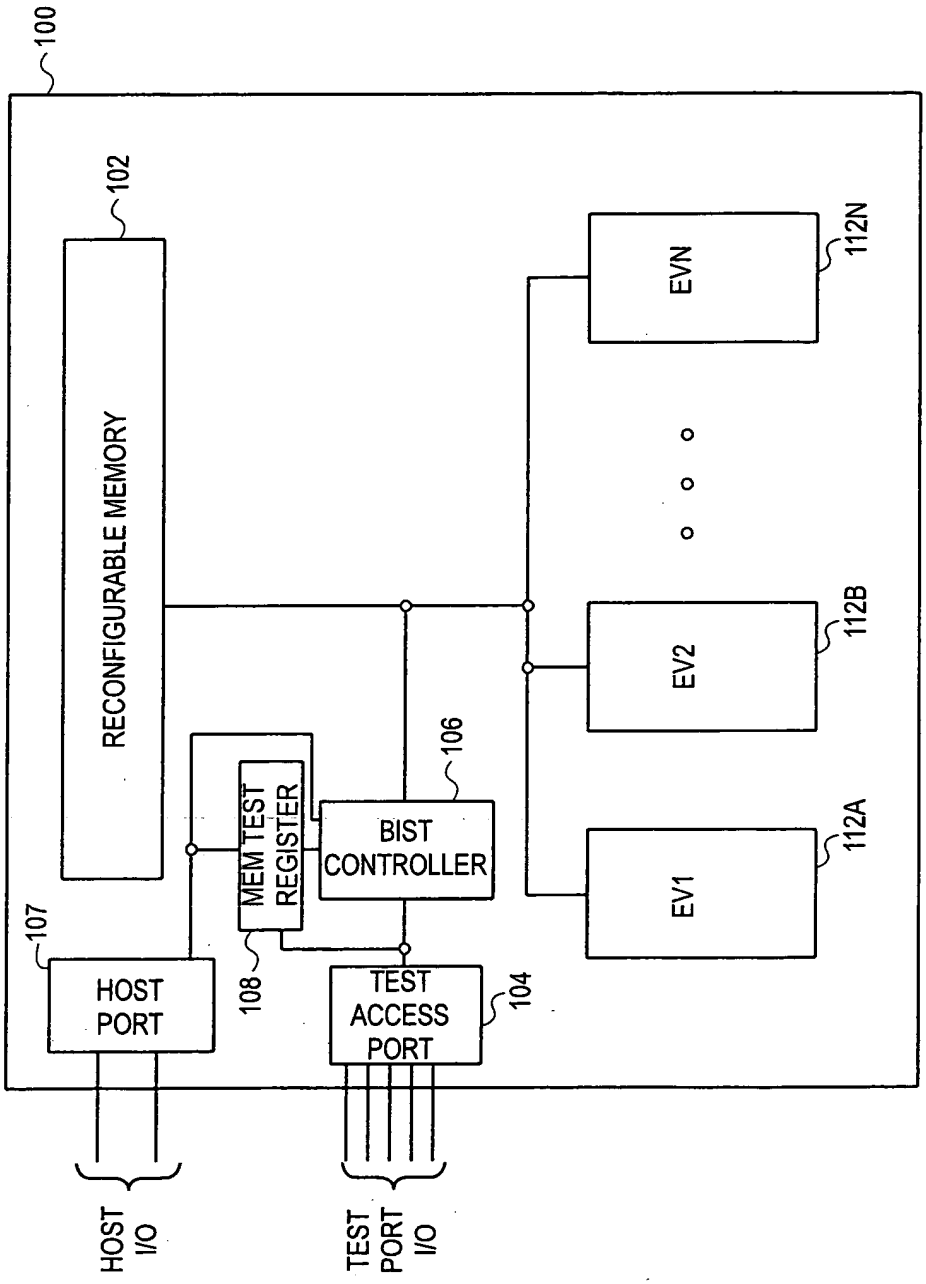

FIG. 1

2/7

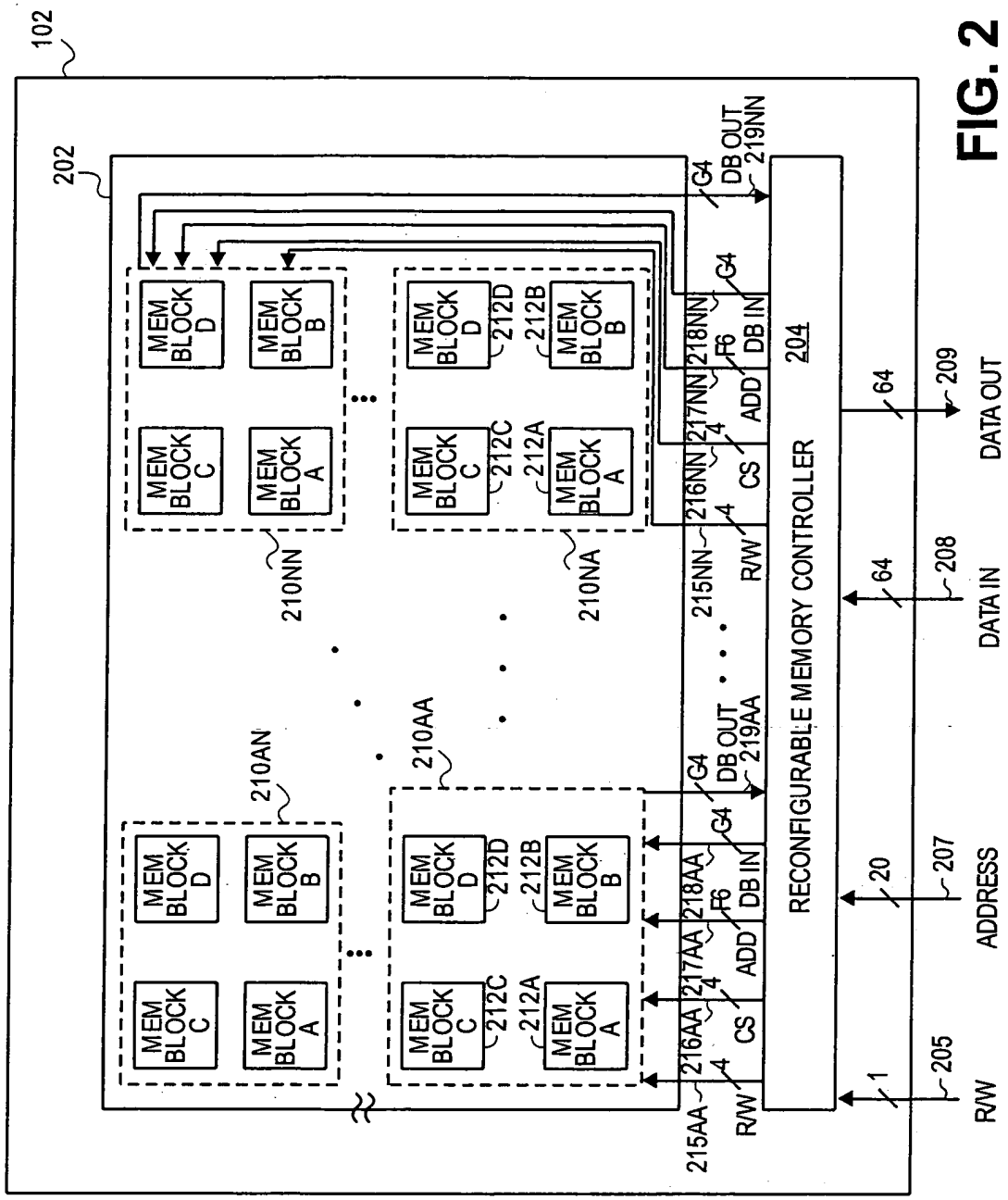
102
202
MEM BLOCK D
MEM BLOCK B
MEM BLOCK C
MEM BLOCK A
212D
212B
212C
212A
210NN
210NA
210AN
210AA
RECONFIGURABLE MEMORY CONTROLLER
204
DB OUT 219NN
DB OUT 219AA
DB IN
ADD
CS
R/W
DATA OUT
DATA IN
ADDRESS
R/W
64
64
20
1
209
208
207
205
G4
F6
4
215NN
215AA
216NN
216AA
217NN
217AA
218NN
218AA

FIG. 2

LOGICAL ADDRESS
ADDRESS MAPPING WITH MAP OUT
PHYSICAL ADDRESS

FIG. 3

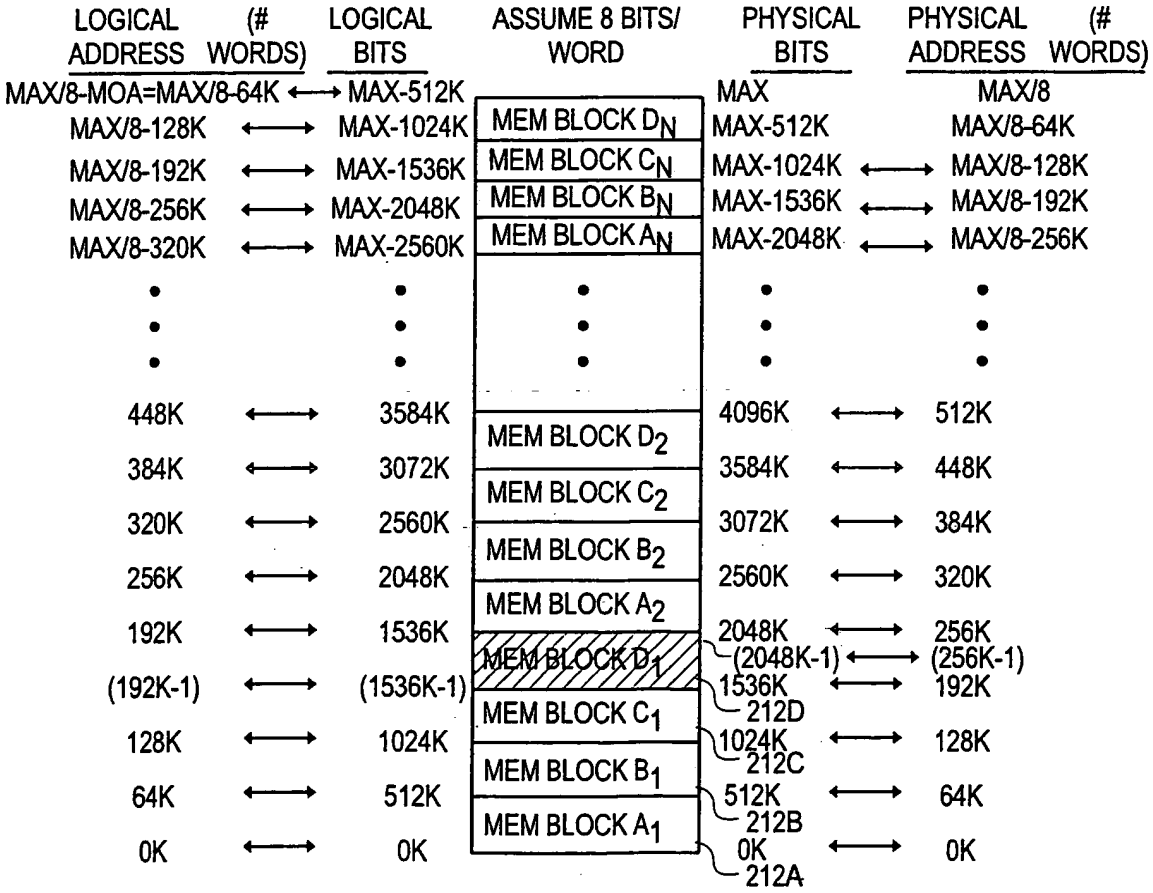
LOGICAL ADDRESS
(# WORDS)
LOGICAL BITS
ASSUME 8 BITS/ WORD
PHYSICAL BITS
PHYSICAL ADDRESS
(# WORDS)
MAX/8-MOA=MAX/8-64K
MAX-512K
MAX
MAX/8
MAX/8-128K
MAX-1024K
MAX-512K
MAX/8-64K
MAX/8-192K
MAX-1536K
MAX-1024K
MAX/8-128K
MAX/8-256K
MAX-2048K
MAX-1536K
MAX/8-192K
MAX/8-320K
MAX-2560K
MAX-2048K
MAX/8-256K
448K
3584K
4096K
512K
384K
3072K
3584K
448K
320K
2560K
3072K
384K
256K
2048K
2560K
320K
192K
1536K
2048K
256K
(192K-1)
(1536K-1)
(2048K-1)
(256K-1)
128K
1024K
64K
512K
0K
0K
MEM BLOCK D_N
MEM BLOCK C_N
MEM BLOCK B_N
MEM BLOCK A_N
MEM BLOCK D_2
MEM BLOCK C_2
MEM BLOCK B_2
MEM BLOCK A_2
MEM BLOCK D_1
MEM BLOCK C_1
MEM BLOCK B_1
MEM BLOCK A_1
1536K
212D
1024K
212C
512K
212B
0K
212A

FIG. 4

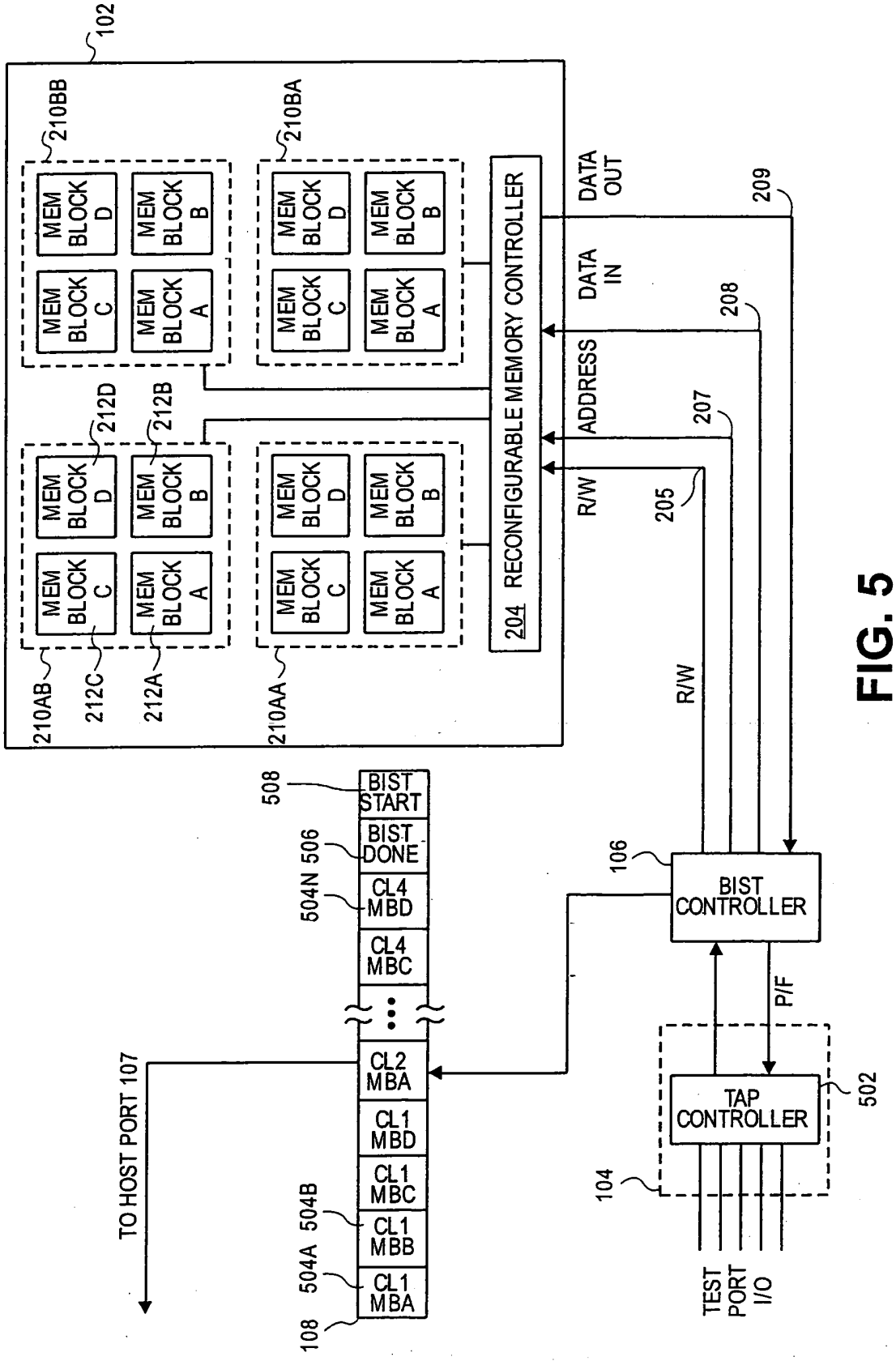
102
210BB
210BA
MEM BLOCK D
MEM BLOCK B
MEM BLOCK C
MEM BLOCK A
212D
212B
212C
212A
210AB
210AA
204 RECONFIGURABLE MEMORY CONTROLLER
DATA OUT
DATA IN
ADDRESS
R/W
209
208
207
205
R/W
508
BIST START
506
BIST DONE
504N
CL4 MBD
CL4 MBC
CL2 MBA
CL1 MBD
CL1 MBC
504B
CL1 MBB
504A
CL1 MBA
108
TO HOST PORT 107
106
BIST CONTROLLER
P/F
TAP CONTROLLER
502
104
TEST PORT I/O

FIG. 5

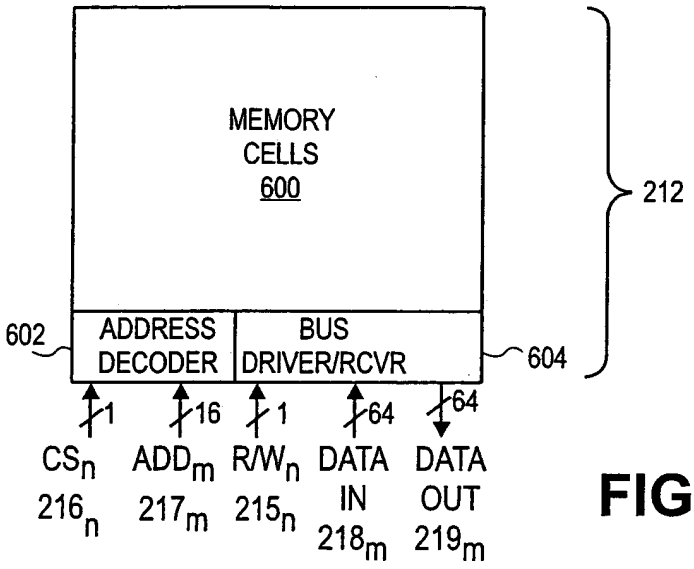
MEMORY
CELLS
600
212
602
ADDRESS
DECODER
BUS
DRIVER/RCVR
604
1
16
1
64
64
CSn
216n
ADDm
217m
R/Wn
215n
DATA
IN
218m
DATA
OUT
219m

FIG. 6

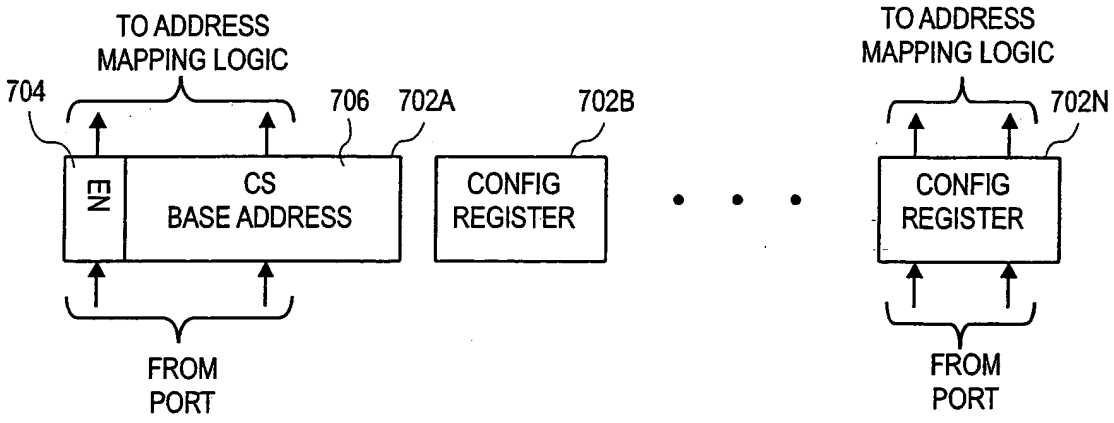
TO ADDRESS
MAPPING LOGIC
704
706
702A
702B
EN
CS
BASE ADDRESS
CONFIG
REGISTER
FROM
PORT
TO ADDRESS
MAPPING LOGIC
702N
CONFIG
REGISTER
FROM
PORT

FIG. 7

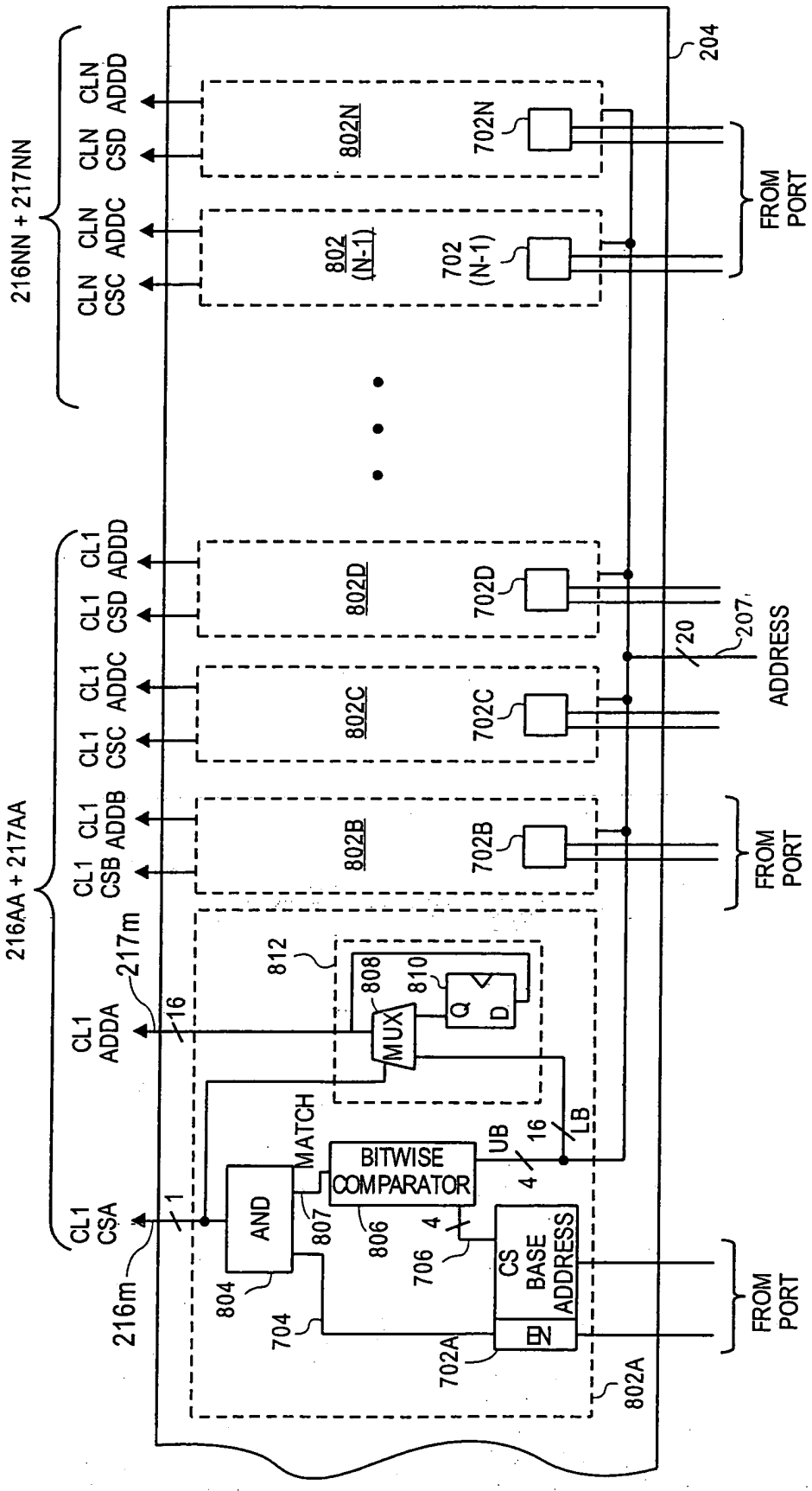
216NN + 217NN
CLN ADDD
CLN CSD
CLN ADDC
CLN CSC
802N
702N
802 (N-1)
702 (N-1)
204
FROM PORT
216AA + 217AA
CL1 ADDD
CL1 CSD
CL1 ADDC
CL1 CSC
CL1 ADDB
CL1 CSB
802D
702D
802C
702C
802B
702B
20
207
ADDRESS
217m
CL1 ADDA
16
812
808
810
MUX
Q
D
MATCH
BITWISE COMPARATOR
UB
LB
16
4
CL1 CSA
1
AND
807
806
706
4
CS
BASE ADDRESS
EN
804
704
702A
802A
216m

FIG. 8

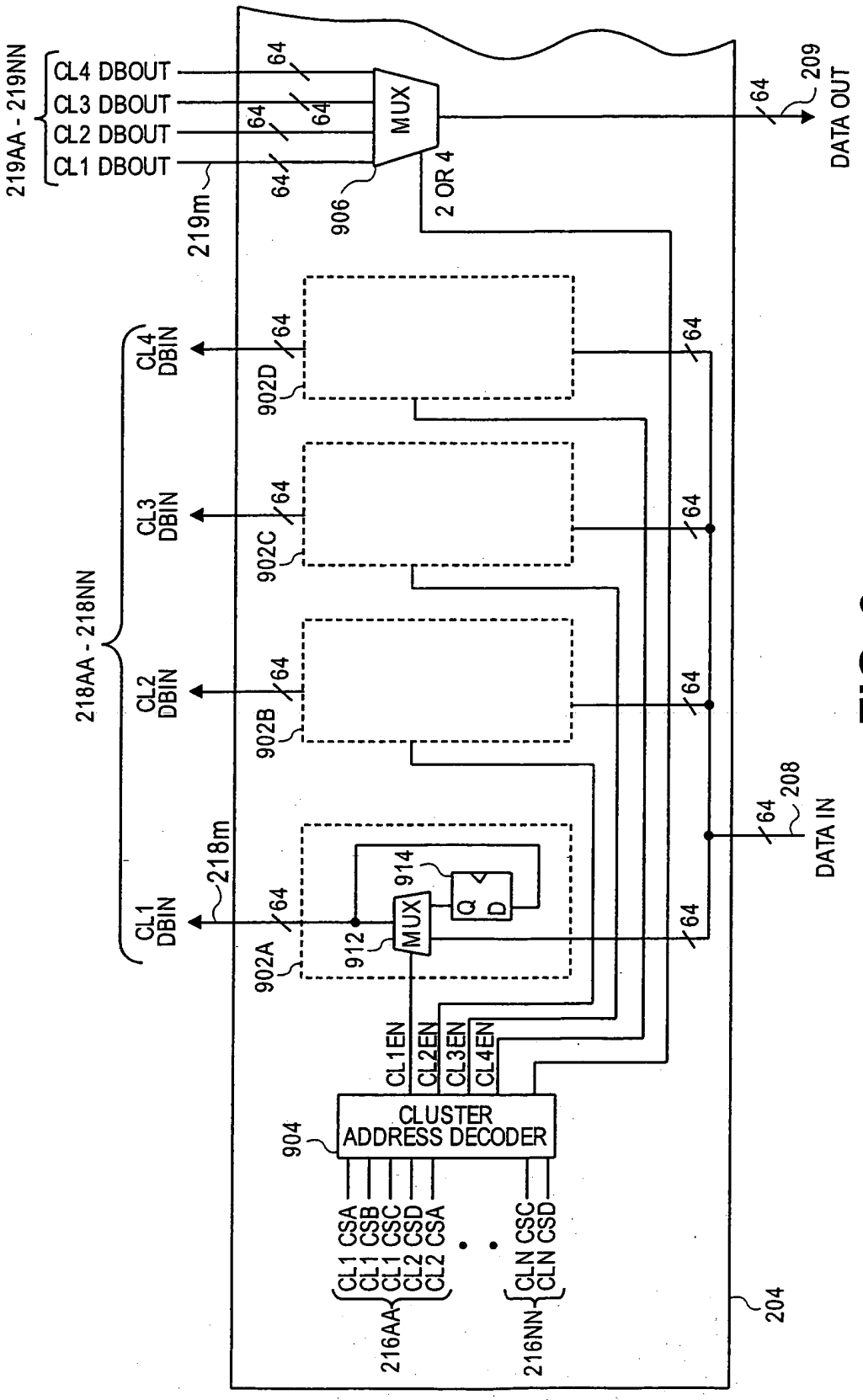
219AA - 219NN
CL4 DBOUT
CL3 DBOUT
CL2 DBOUT
CL1 DBOUT
64
MUX
2 OR 4
906
219m
209
DATA OUT
218AA - 218NN
CL4 DBIN
CL3 DBIN
CL2 DBIN
CL1 DBIN
902D
902C
902B
902A
218m
914
912
Q
D
208
DATA IN
CL1EN
CL2EN
CL3EN
CL4EN
CLUSTER ADDRESS DECODER
904
CL1 CSA
CL1 CSB
CL1 CSC
CL2 CSD
CL2 CSA
CLN CSC
CLN CSD
216AA
216NN
204

FIG. 9